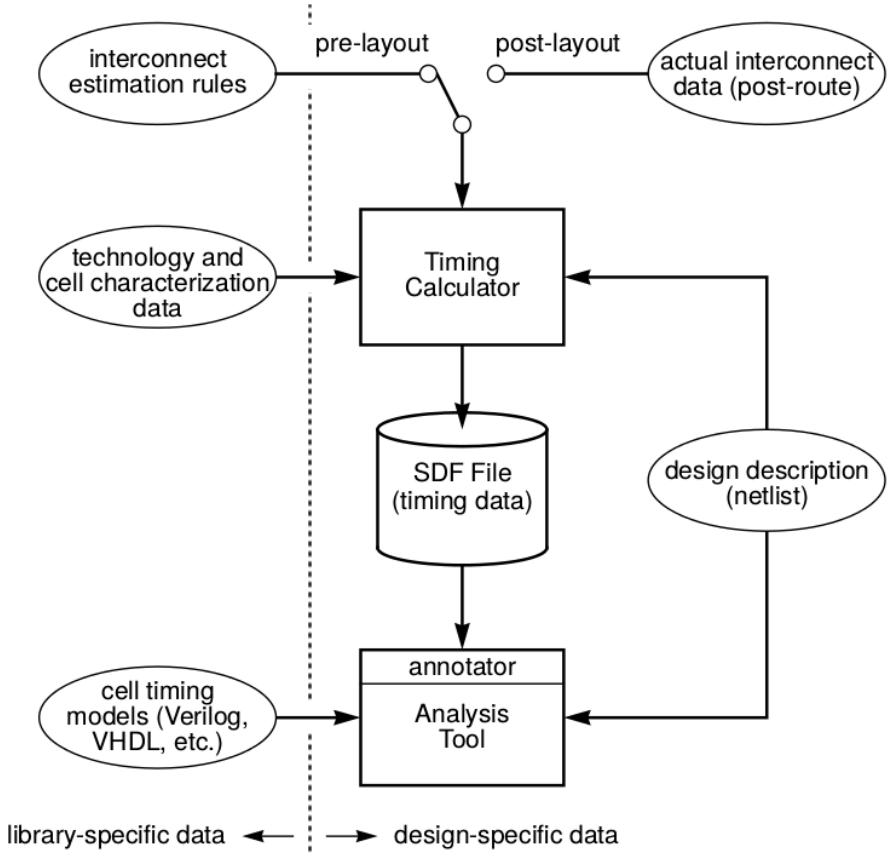
SDF (Standard Delay Format) (H.1)

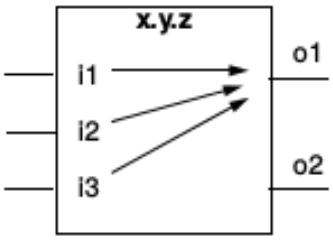
20151201

References

Standard Delay Format Specification
Version 3.0
May 1995
Open Verilog International

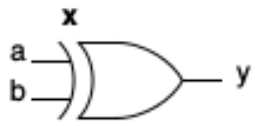
Figure 2 SDF Files in Timing Back-Annotation





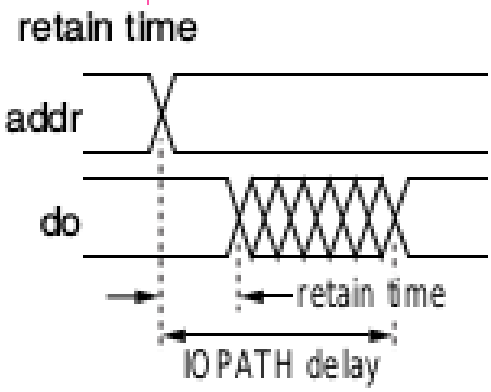
Example

```
(INSTANCE x.y.z)
(DELAY
  (ABSOLUTE
    (IOPATH (posedge i1) o1 (2:3:4) (4:5:6))
    (IOPATH i2 o1 (2:4:5) (5:6:7))
    (IOPATH i3 o1 () () (2:4:5) (4:5:6) (2:4:5) (4:5:6))
  )
)
```



Example

```
(INSTANCE x)
(DELAY
  (ABSOLUTE
    (COND b  (IOPATH a y (0.21) (0.54) ) )
    (COND ~b (IOPATH a y (0.27) (0.34) ) )
    (COND a  (IOPATH b y (0.42) (0.44) ) )
    (COND ~a (IOPATH b y (0.37) (0.45) ) )
  )
)
```

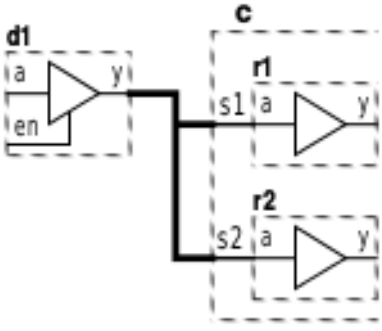


strictly monotonically increasing.

Example

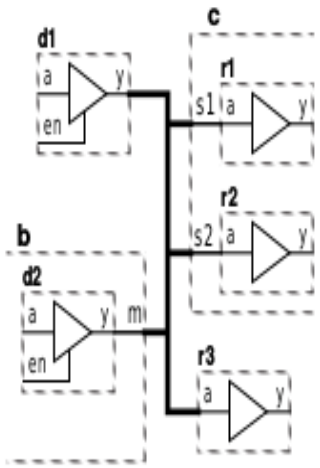
```
(IOPATH addr[13:0] do[7:0]
  (RETAIN (4:5:7) (5:6:9))
```

delval_list is the **PORT** delay of the *port_instance*.



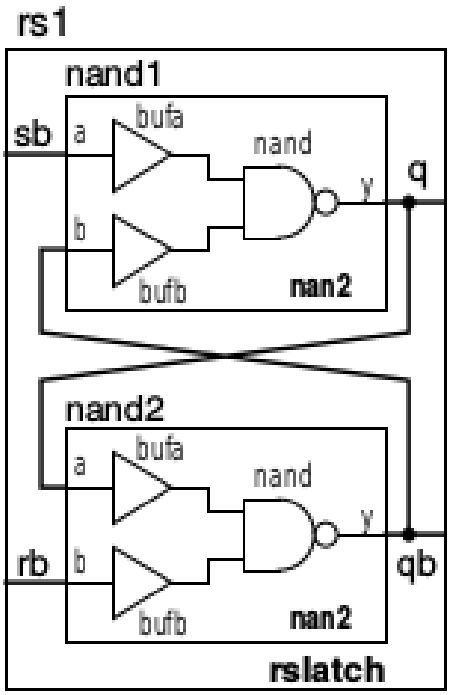
Example

```
(INSTANCE c)
(DELAY
  (ABSOLUTE
    (PORT r1.a (0.01:0.02:0.03))
    (PORT r2.a (0.03:0.04:0.05))
  )
```



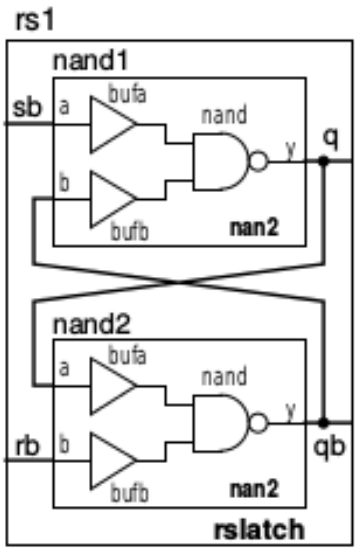
Example

```
(INSTANCE top)
(DELAY
  (ABSOLUTE
    (INTERCONNECT  d1.y   c.r1.a (0.01:0.02:0.03))
    (INTERCONNECT  d1.y   c.r2.a (0.03:0.04:0.05))
    (INTERCONNECT  d1.y   r3.a   (0.05:0.06:0.07))
    (INTERCONNECT  b.d2.y c.r1.a (0.04:0.05:0.06))
    (INTERCONNECT  b.d2.y c.r2.a (0.02:0.03:0.04))
    (INTERCONNECT  b.d2.y r3.a   (0.02:0.03:0.04))
  )
)
```



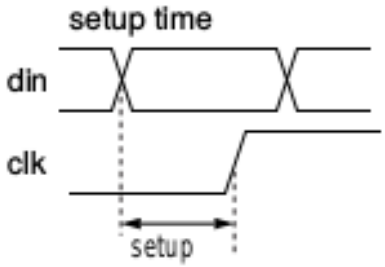
Example

```
(CELL
  (CELLTYPE "buf")
  (INSTANCE rs1.nand1.bufa)
  (DELAY
    (ABSOLUTE
      (DEVICE (1:3:8) (4:5:7))
    )
  )
)
(CELL
  (CELLTYPE "buf")
  (INSTANCE rs1.nand1.bufb)
  (DELAY
    (ABSOLUTE
      (DEVICE (2:4:9) (6:8:12))
    )
  )
)
```



Example

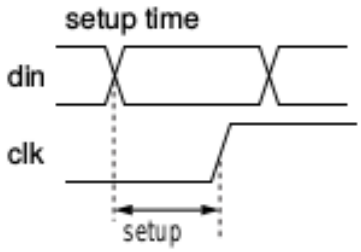
```
(CELL
  (CELLTYPE "buf")
  (INSTANCE rs1.nand1.bufa)
  (DELAY
    (ABSOLUTE
      (DEVICE (1:3:8) (4:5:7))
    )
  )
)
(CELL
  (CELLTYPE "buf")
  (INSTANCE rs1.nand1.bufb)
  (DELAY
    (ABSOLUTE
      (DEVICE (2:4:9) (6:8:12))
    )
  )
)
```



not be negative.

Example

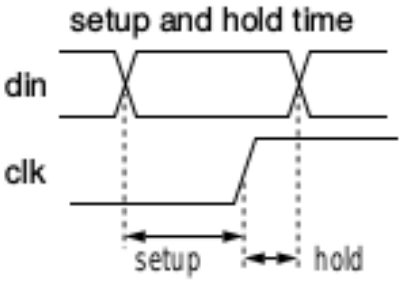
```
(INSTANCE x.a)
(TIMINGCHECK
  (SETUP din (posedge clk) (12))
)
```



not be negative.

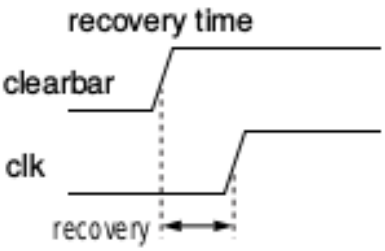
Example

```
(INSTANCE x.a)
(TIMINGCHECK
  (SETUP din (posedge clk) (12))
)
```



Example

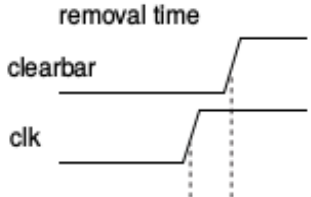
```
(INSTANCE x.a)
(TIMINGCHECK
  (SETUPHOLD (COND ~reset din) (posedge clk)
)
```



Example

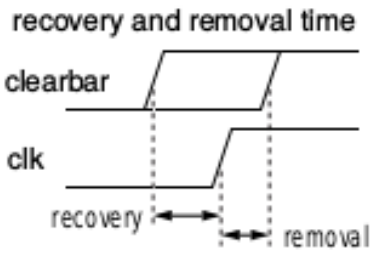
```
(INSTANCE x.b)
(TIMINGCHECK
  (RECOVERY (posedge clearbar) (posedge clk) (
)
```

of new data.



Example

```
(INSTANCE x.b)
(TIMINGCHECK
  (REMOVAL (posedge clearbar) (posedge clk) (6.3))
```

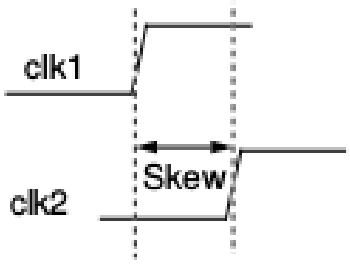


26.

Example

```
(INSTANCE x.b)
(TIMINGCHECK
  (RECREM (posedge clearbar) (posedge clk) (1.5) (0.8)
)
```

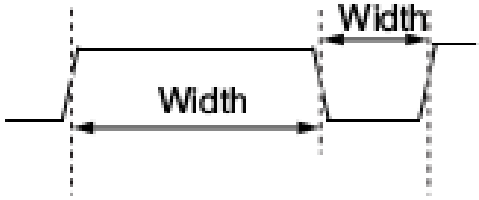
This example specifies a recovery time of 1.5 and a removal time of 0.8



Example

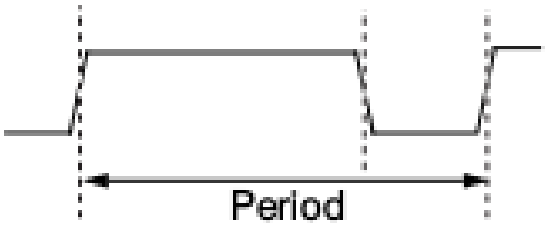
```
(INSTANCE x)
(TIMINGCHECK
  (SKEW (posedge clk1) (posedge clk2) (6))
)
```

As with all *port_tchks*, the **COND** construct can be used



Example

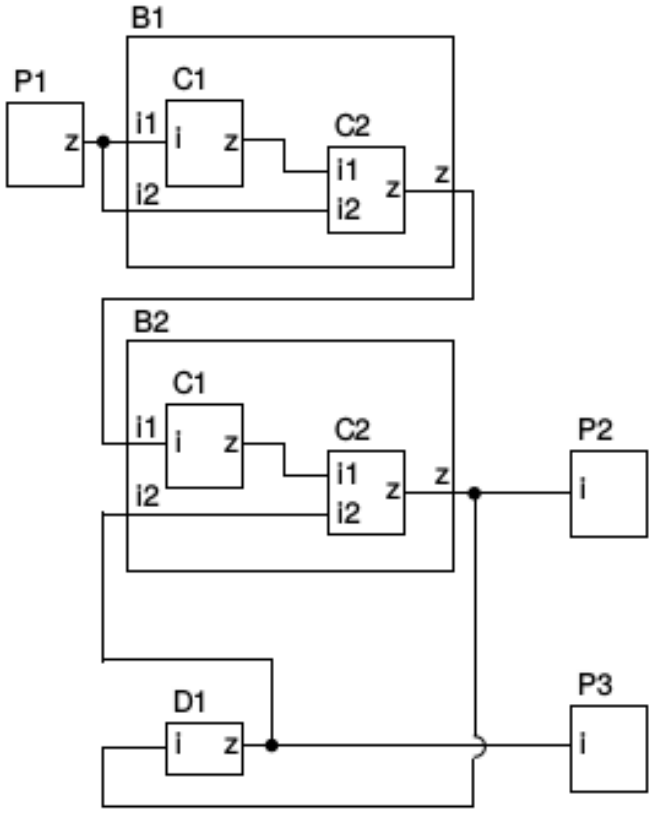
```
(INSTANCE x.b)
(TIMINGCHECK
  (WIDTH (posedge clk) (30))
  (WIDTH (negedge clk) (16.5))
)
```



Example

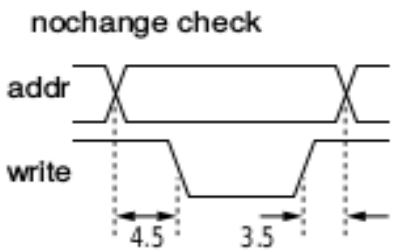
```
(INSTANCE x.b)
(TIMINGCHECK
  (PERIOD (posedge clk) (46.5))
```

Figure 4 SDF Example Schematic




```
(DELAYFILE
  (SDFVERSION "1.0")
  (DESIGN "system")
  (DATE "Saturday September 30 08:30:33 PST 1990")
  (VENDOR "Yosemite Semiconductor")
  (PROGRAM "delay_calc")
  (VERSION "1.5")
  (DIVIDER /)
  (VOLTAGE 5.5:5.0:4.5)
  (PROCESS "worst")
  (TEMPERATURE 55:85:125)
  (TIMESCALE 1ns)
  (CELL
    (CELLTYPE "system")
    (INSTANCE )
    (DELAY
      (ABSOLUTE
        (INTERCONNECT P1/z     B1/C1/i   (.145::.145) (.125::.125))
        (INTERCONNECT P1/z     B1/C2/i2  (.135::.135) (.130::.130))
        (INTERCONNECT B1/C1/z  B1/C2/i1  (.095::.095) (.095::.095))
```

```
        (INTERCONNECT B1/C2/z B2/C1/i  (.145::.145) (.125::.125))
        (INTERCONNECT B2/C1/z B2/C2/i1 (.075::.075) (.075::.075))
        (INTERCONNECT B2/C2/z P2/i     (.055::.055) (.075::.075))
        (INTERCONNECT B2/C2/z D1/i     (.255::.255) (.275::.275))
        (INTERCONNECT D1/z    B2/C2/i2 (.155::.155) (.175::.175))
        (INTERCONNECT D1/z    P3/i     (.155::.155) (.130::.130))
      )
    )
  )
  (CELL
    (CELLTYPE "INV")
    (INSTANCE B1/C1)
    (DELAY
      (ABSOLUTE
        (IOPATH i  z (.345::.345) (.325::.325) )
      )
    )
  )
  (CELL
    (CELLTYPE "OR2")
    (INSTANCE B1/C2)
    (DELAY
      (ABSOLUTE
        (IOPATH i1  z (.300::.300) (.325::.325) )
        (IOPATH i2  z (.300::.300) (.325::.325) )
      )
    )
  )
  (CELL
    (CELLTYPE "INV")
    (INSTANCE B2/C1)
    (DELAY
      (ABSOLUTE
        (IOPATH i  z (.345::.345) (.325::.325) )
      )
    )
  )
  (CELL
    (CELLTYPE "AND2")
    (INSTANCE B2/C2)
    (DELAY
      (ABSOLUTE
        (IOPATH i1  z (.300::.300) (.325::.325) )
        (IOPATH i2  z (.300::.300) (.325::.325) )
      )
    )
  )
  (CELL
    (CELLTYPE "INV")
    (INSTANCE D1)
    (DELAY
      (ABSOLUTE
        (IOPATH i  z (.380::.380) (.380::.380) )
      )
    )
  )
)
```



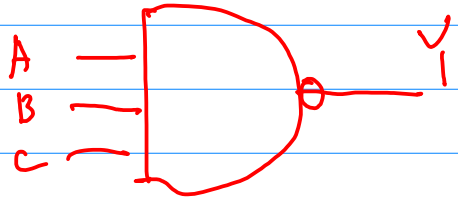
Example

```
(INSTANCE x)
(TIMINGCHECK
  (NOCHANGE (negedge write) addr (4.5) (3.5))
)
```

This example defines a period beginning 4.5 time units before the

Verilog Cell Primitive

```
`timescale 1ns/1ps

`celldefine

module NAND3 (Y, A, B, C);
  output Y;
  input  A, B, C;

  // Use Verilog NAND primitive
  nand (Y, A, B, C);

  specify
    // delay parameters
    specparam tr = 1.0,  tf = 1.0;

    // path delayss
    (A *> Y) = (tr, tf);
    (B *> Y) = (tr, tf);
    (C *> Y) = (tr, tf);
  endspecify

endmodule

`endcelldefine
```



annotated delay example

```
(DELAYFILE
 (DESIGN "TESTING")
 (TIMESCALE 1ns)
 (CELL
  (CELLTYPE "NAND3")
  (INSTANCE *) // Any NAND3
  (DELAY
    (ABSOLUTE
      (IOPATH A Y (0.1965:0.2863:0.4268) (0.2101:0.3294:0.5626))
      (IOPATH B Y (0.1935:0.2783:0.4079) (0.2281:0.3477:0.5740))
      (IOPATH C Y (0.1648:0.3614:0.4763) (0.2795:0.4372:0.7556))
    )
  )
 )
)
```

http://www2.ece.ohio-state.edu/~bibyk/ee683/BolinM_part2_timing.pdf

```
`timescale 1ns/1ps

`celldefine

module DFF (QP, QN, D, CLK);
  output   QP, QN;
  input    D, CLK;
  reg      NOTIFIER;
  supply1 RN, SN;

  buf             I3 (clk, CLK);
  udp_dff         I0 (n0, D, clk, RN, SN, NOTIFIER);
  and             I4 (flag, RN, SN);
  buf             I1 (QP, n0);
  not             I2 (QN, n0);

  specify
    specparam
      trcq  = 1.0,     tfcq  = 1.0,     trcqn     = 1.0,     tfcqn     = 1.0,
      tset  = 1.0,     thld  = 1.0,     tmaxpw    = 1.0,     tminpw    = 1.0;

      // PATH DELAYS
      if (flag) (posedge CLK *> (QP   +: D)) = (trcq, tfcq);
      if (flag) (posedge CLK *> (QN   -: D)) = (trcqn, tfcqn);
      $setuphold (posedge CLK &&& (flag == 1), posedge D, tset, thld, NOTIFIER);
      $setuphold (posedge CLK &&& (flag == 1), negedge D,  tset, thld, NOTIFIER);
      $width(negedge CLK, tminpw, 0, NOTIFIER);
      $width(posedge CLK, tminpw, 0, NOTIFIER);
  endspecify

endmodule

`endcelldefine
```

http://www2.ece.ohio-state.edu/~bibyk/ee683/BolinM_part2_timing.pdf

UDP (User Defined Primitive)

```
primitive udp_dff (out, in, clk, clr_, set_, NOTIFIER);
   output  out;
   input        in, clk, clr_, set_, NOTIFIER;
   reg     out;

   table

//       |---------------------------------- in
//       |   |---------------------------------- clk
//       |   |    |---------------------------- clr_
//       |   |    |    |----------------------- set_
//       |   |    |    |    |------------------- NOT
//       |   |    |    |    |      |------------- Qt
//       |   |    |    |    |      |      |-------- Qt+1
//       |   |    |    |    |      |      |
//       |   |    |    |    |      |      |
//       |   |    |    |    |      |      |
//       |   |    |    |    |      |      |
         0   r    ?    1    ?    : ?  :  0  ; // clock in 0
         1   r    1    ?    ?    : ?  :  1  ; // clock in 1
         1   *    1    ?    ?    : 1  :  1  ; // reduce pessimism
         0   *    ?    1    ?    : 0  :  0  ; // reduce pessimism
         ?   f    ?    ?    ?    : ?  :  -  ; // no changes on negedge clk
         *   b    ?    ?    ?    : ?  :  -  ; // no changes when in switches
         ?   ?    ?    0    ?    : ?  :  1  ; // set output
         ?   b    1    *    ?    : 1  :  1  ; // cover all transistions on set_
         1   x    1    *    ?    : 1  :  1  ; // cover all transistions on set_
         ?   ?    0    1    ?    : ?  :  0  ; // reset output
         ?   b    *    1    ?    : 0  :  0  ; // cover all transistions on clr_
         0   x    *    1    ?    : 0  :  0  ; // cover all transistions on clr_
         ?   ?    ?    ?    *    : ?  :  x  ; // any notifier changed

   endtable

endprimitive
```

http://www2.ece.ohio-state.edu/~bibyk/ee683/BolinM_part2_timing.pdf

STATE	Description
0	Logic low
1	Logic high
X	Unknown
Z	High impedance
?	0 or 1 or X
b	0 or 1
f	(1-0), Falling Edge on an input
r	(0-1), Rising Edge on an input
p	(0-1) or (0-x) or (x-1) or (1-z) or (z-1)
n	(1-0) or (1-x) or (x-0) or (0-z) or (z-0)
*	(??), All transitions
-	No Change

http://www2.ece.ohio-state.edu/~bibyk/ee683/BolinM_part2_timing.pdf

annotated delay example

```
(DELAYFILE
 (DESIGN "TESTING")
 (TIMESCALE 1ns)
 (CELL
   (CELLTYPE "DFF")
   (INSTANCE *) // Any DFF
   (DELAY
     (ABSOLUTE
     (IOPATH (posedge CLK) QP (0.32:0.48:0.73) (0.2:0.43:0.67))
     (IOPATH (posedge CLK) QN (0.32:0.48:0.73) (0.2:0.4:0.6))
     (IOPATH  D QP (0.1:0.2:0.3) (0.1:0.2:0.4))
     (IOPATH  D QN (0.1:0.2:0.3) (0.1:0.2:0.4))))
   (TIMINGCHECK
     (HOLD (posedge D) (posedge CLK) (0.1433:0.1818:0.2228))
     (HOLD (negedge D) (posedge CLK) (0.0580:0.0646:0.0800))
     (SETUP (posedge D) (posedge CLK) (0.0705:0.0411:0.0020))
     (SETUP (negedge D) (posedge CLK) (0.1556:0.1525:0.1464))
     (WIDTH (negedge CLK) (0.1230:0.1780:0.2700))
     (WIDTH (posedge CLK) (0.1650:0.2460:0.3890))
   )
 )
)
```